AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A clock generator comprising:

an input;

an output;

an oscillator that generates a reference clock, and

a phase control means that receives the reference clock, controls a phase of the reference clock according to a variable setting condition at each clock cycle, and generates a phase controlled clock, comprising a first charge pump, a delay setting circuit that is responsive to said phase control means, and a second charge pump that receives the output of said delay setting circuit,

wherein the phase control means varies a setting condition to spread a spectrum of the phase controlled clock outputted at said output.

2. (currently amended): A clock generator comprising:

a phase control means that receives a ~~the~~ reference clock and~~,~~ controls a phase of the reference clock according to a variable setting condition at each clock cycle, and generates a phase controlled clock, said phase control means comprising a first charge pump, a delay setting circuit, and a second charge pump that receives the output of said delay setting circuit,

wherein the phase control means varies a setting condition to spread a spectrum of the phase controlled clock outputted at said output.

3. (currently amended): A clock generator as claimed in Claim 1, wherein ~~the phase control means includes~~ said variable delay circuit ~~that~~ delays the reference clock to comply with a control input according to the setting condition, and said phase control means includes a circuit that detects a delayed state in the variable delay circuit, and regulates the control input to the variable delay circuit in such a manner that a phase difference of the phase controlled clock to

the reference clock does not exceed a specific limit value defined by the reference clock cycle as a unit.

4. (currently amended): A clock generator as claimed in Claim 1, wherein the phase control means regulates the control input according to such a profile that the phase difference of the phase controlled clock to the reference clock gradually increases and gradually decreases between the upper limit and lower limit of the specific limit value defined by the reference clock cycle as a unit.

5. (currently amended): A clock generator as claimed in Claim 3, wherein said phase control means comprises ~~comprising~~ a DLL circuit containing the variable delay circuit as a circuit element, wherein the ~~DLL circuit and the~~ phase control means synthesizes the control input to the variable delay circuit.

6. (currently amended): A clock generator ~~as claimed in Claim 5,~~ comprising:

an input;

an output;

an oscillator that generates a reference clock, and

a phase control means that receives the reference clock, controls a phase of the reference clock according to a variable setting condition at each clock cycle, and generates a phase controlled clock,

wherein the phase control means varies a setting condition to spread a spectrum of the phase controlled clock outputted at said output,

wherein the phase control means includes (1) a variable delay circuit that delays the reference clock to comply with a control input according to the setting condition, (2) a circuit that detects a delayed state in the variable delay circuit and regulates the control input to the variable delay circuit in such a manner that a phase difference of the phase controlled clock to the reference clock does not exceed a specific limit value defined by the reference clock cycle as a unit, and (3) a DLL circuit containing the variable delay circuit as a circuit element, wherein phase control means synthesizes the control input to the variable delay circuit, and wherein:

the variable delay circuit ~~is served as a circuit that~~ delays the reference clock based on a control voltage;

the DLL circuit includes a comparator that compares the phase of a delayed output clock from the variable delay circuit and the phase of the reference clock, and a first charge pump that generates the control voltage to the variable delay circuit according to a phase difference output from the comparator; and

the phase control means uses a second charge pump of which capacity is greater than that of the first charge pump in a circuit for adjusting the control input, and generates the control voltage according to a phase difference set as a control condition.